APPENDIX

(37 C.F.R. § 1.192(c)(9))

The following claims are involved in this appeal:

1. A method for controlling operation of a multi-pair gigabit transceiver, the multi-pair gigabit transceiver comprising a Physical Layer control module (PHY control module), a Physical Coding Sublayer module (PCS module) and a digital signal processing module (DSP), the method comprising:

receiving at the PHY control module user-defined inputs from a serial management module and status signals from the DSP and the PCS module;

generating, at the PHY control module, control signals responsive to the user-defined inputs and the status signals; and

providing the control signals to the DSP and the PCS module.

2. The method of Claim 1 wherein the multi-pair gigabit transceiver further comprises an auto-negotiation module, the method further comprising:

receiving at the PHY control module a link control signal from the auto-negotiation module to start operation of the PCS module and the DSP.

3. The method of Claim 1 wherein the multi-pair gigabit transceiver further comprises a Gigabit Medium Independent Interface (GMII) module, the method further comprising:

receiving at the PHY control module a transmit enable signal from the GMII module to start transmission of data packets.

4. The method of Claim 1 further comprising:

receiving a user-defined reset signal at the PHY control module; and

generating a control signal to reset the DSP and the PCS module.

5. The method of Claim 1 wherein the control signals include a DSP/PCS reset signal to reset the DSP and the PCS module.

6. The method of Claim 1 wherein the DSP comprises a set of echo cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the control signals include echo and NEXT control signals to control convergence of the echo cancellers and NEXT cancellers, respectively.

7. The method of Claim 1 wherein the DSP comprises a multi-dimensional decision feedback equalizer (DFE) and wherein the control signals include DFE control signals to control convergence of the multi-dimensional DFE.

8. The method of Claim 1 wherein the DSP comprises a timing recovery (TR) module and wherein the control signals include TR control signals to control convergence of the timing recovery module.

15. A PHY control module for controlling operation of a multi-pair Ethernet transceiver, the multi-pair Ethernet transceiver comprising a Physical Coding Sublayer module (PCS module) and a Digital Signal Processing module (DSP), the PHY control module comprising:

a main state machine configured to receive user-defined inputs from a serial management module and status signals from the DSP and the PCS module, to generate control signals responsive to the user-defined inputs and the status signals, and to provide the control signals to the DSP and the PCS module.

16. The PHY control module of Claim 15 wherein the multi-pair Ethernet transceiver further comprises an auto negotiation module and wherein the main state machine receives a link control signal from the auto negotiation module to start operation of the PCS module and the DSP.

17. The PHY control module of Claim 15 wherein the multi-pair Ethernet transceiver further comprises a Gigabit Medium Independent Interface (GMII) module and wherein the main state machine receives a transmit enable signal from the GMII module to start transmission of data packets.

18. The PHY control module of Claim 15 wherein the main state machine receives a user-defined reset signal and generates a control signal to reset the DSP and the PCS module.

19. The PHY control module of Claim 15 wherein the control signals include a DSP/PCS reset signal to reset the DSP and the PCS module.

20. The PHY control module of Claim 15 wherein the DSP comprises a set of echo cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the control signals include echo and NEXT control signals to control convergence of the echo cancellers and NEXT cancellers, respectively.

21. The PHY control module of Claim 15 wherein the DSP comprises a multi-dimensional decision feedback equalizer (DFE) and wherein the control signals include DFE control signals to control convergence of the multi-dimensional DFE.

22. The PHY control module of Claim 15 wherein the DSP comprises a timing recovery (TR) module and wherein the control signals include TR control signals to control convergence of the timing recovery module.